
Retrospective Theses and Dissertations

1976

A Differential Sample and Hold Technique that Rejects Offset Voltages

John Adams Davis
University of Central Florida

 Part of the [Engineering Commons](#)

Find similar works at: <https://stars.library.ucf.edu/rtd>

University of Central Florida Libraries <http://library.ucf.edu>

This Masters Thesis (Open Access) is brought to you for free and open access by STARS. It has been accepted for inclusion in Retrospective Theses and Dissertations by an authorized administrator of STARS. For more information, please contact STARS@ucf.edu.

STARS Citation

Davis, John Adams, "A Differential Sample and Hold Technique that Rejects Offset Voltages" (1976). *Retrospective Theses and Dissertations*. 208.
<https://stars.library.ucf.edu/rtd/208>

78-190

A DIFFERENTIAL SAMPLE AND HOLD TECHNIQUE
THAT REJECTS OFFSET VOLTAGES

BY

JOHN ADAMS DAVIS, JR.
B.S.E.E., North Carolina State University, 1971

RESEARCH REPORT

Submitted in partial fulfillment of the requirements
for the degree of Master of Engineering
in the Graduate Studies Program of
Florida Technological University, 1976

Orlando, Florida

ABSTRACT

A DIFFERENTIAL SAMPLE AND HOLD TECHNIQUE THAT REJECTS OFFSET VOLTAGES

BY

JOHN ADAMS DAVIS, JR.

This research report discusses modern sample and hold theory and techniques and then uses them to develop a new differential sampling concept to solve a real engineering problem, involving the synchronous demodulation of three amplitude modulated direction cosine signals in an unusual noise environment. The problem is discussed in detail and a detailed circuit design solution given. Additionally, the results of a breadboard test of the concept is given that shows the circuit to have a 60dB offset voltage rejection ratio.

ACKNOWLEDGMENTS

The author wishes to express his sincere gratitude to his advisor and committee chairman, Dr. Richard C. Harden, for his help and guidance not only during the preparation of this research report, but also at every step of the long post-graduate studies road. He is also thankful to Mrs. Marie Farmer for the many hours she spent in typing this report.

This research report is dedicated to the author's wonderful wife, Sharon, without whose encouragement, love and patience this paper would not have been written, nor would any post-graduate studies have been possible.

TABLE OF CONTENTS

ACKNOWLEDGMENTS.....	iii
INTRODUCTION.....	1
CHAPTER I SAMPLE AND HOLD THEORY AND TECHNIQUES....	5
CHAPTER II THE PROBLEM TO BE SOLVED.....	14
The System.....	14
The Interface Subsystem.....	16
The Error Budget.....	17
The Input Signals.....	20
The Synchronous Demodulator —	
Our Design Problem.....	22
CHAPTER III THE CIRCUIT DESIGN.....	26
The Input Stage.....	28
The Sample and Hold Stage.....	31
The Error Total.....	42
The Breadboard Circuit.....	44
Conclusions.....	46
BIBLIOGRAPHY.....	47

INTRODUCTION

An airborne fire control system (machine aid for accurate weapon delivery) has been designed, built and flight tested against ground targets. This system searches out and "locks on" to coded pulses of light that reflect from laser designated (illuminated) targets (the laser designator apparatus is operated from either the ground or another aircraft). Once "lock on" is effected, the system continually informs an on board digital computer of the precise angular target location with respect to the airframe co-ordinates. The computer, in turn, generates steering commands and computes the optimum weapons (bombs, rockets or gunfire) release or firing position/time to facilitate the accurate delivery of ordnance on the target. The accuracies involved in this system are such that, in most cases, it will no longer be necessary to utilize unconventional and expensive weaponry such as "smart" bombs or homing rockets to facilitate precise weapon delivery.

The system consists of an external (mounted outside of the aircraft skin) pod with a gimbaled seeker mechanism, an aircraft interface unit (AIU), and an

on board digital computer. When "lock on" occurs, the seeker mechanism "looks" (points) in the direction of the target. The gimbal angular positions with respect to the airframes structural co-ordinates are precisely determined and electrical representations of the angles are output as amplitude modulated A.C. signals (resolver position signals). The AIU converts these analog signals to digital angular representations in a format acceptable for use by the digital airborne computer. The computer uses the angular information to generate steering commands to be used by the pilot or an automatic flight control system. It also computes the optimum point and time at which to release/fire the selected weapons.

The system flight tests were very successful except for one important problem. It was discovered that the output from the external pod had an unusual noise added to the analog signals that contain the angular target location information. This noise was not being rejected by the AIU, and, when present, would cause errors in the signals that were much greater than those allowed by the system specifications.

The subject of this paper, then, is a new noise

rejection scheme and the design of the necessary AIU circuitry to implement it. This new design must not only meet the system specifications but also make no unnecessary conceptual changes and should utilize as much of the existing design and components as possible to reduce cost and facilitate the easiest customer approval of the system. With this in mind, it was decided to re-design only the analog input demodulation (sample and hold) circuitry in the AIU.

To help the reader not familiar with sample and hold (S&H) circuitry to understand this report, Chapter I contains a review of basic S&H theory and techniques. Chapter II contains an in depth discussion of the problem to be solved. The design and the design process are presented in Chapter III along with the results of testing the new scheme using a breadboard model of the design.

Certain abbreviations are used in the text of this research report. They are:

S&H	meaning sample and hold circuit(s)
R	meaning resistance or resistor
C	meaning capacitance or capacitor
FET	meaning field effect transistor
OP AMP	meaning operational amplifier
V	meaning volts - steady state

v	meaning volts - instantaneous
I	meaning amperes/current - steady state
i	meaning amperes/current - instantaneous
t	meaning time (in seconds unless otherwise specified)
SFEEC	meaning scale factor error equivalence cancellation
A/D	meaning analog to digital (converter circuit)
RSS	meaning the root of the sum of the squares
exp(x)	meaning the quantity 2.71828 raised to the exponent x
ln(x)	meaning the natural log of the quantity(x)

Subscripts such as $R_{\text{FET-OFF}}$ are used to differentiate between these abbreviations, to clarify them or just to add supplementary information.

CHAPTER I

SAMPLE AND HOLD THEORY AND TECHNIQUES

S&H circuits are used to sample (detect) the value of a signal at a given point in time and hold (remember) that value indefinitely or, until it is desired that the signal value be sampled and held again at another point in time. The basic scheme for S&H circuits is shown in Figure I-1. The memory device follows the input signal (samples) until the switch is changed from the sample to the hold position at which time the memory device causes the signal at the S&H output to remain (hold) at the last known (memorized) value before the switch was opened.

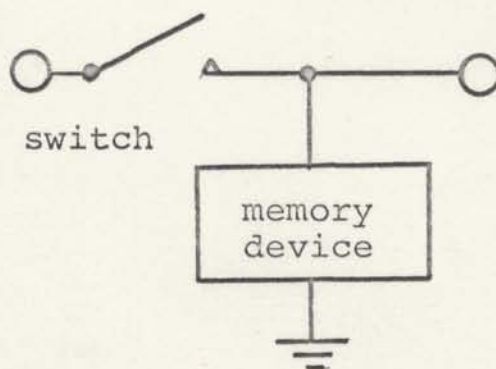


Figure I-1. Basic S&H Scheme

There are many techniques for implementing this scheme using real hardware. However, the most common one used today is shown in Figure I-2.

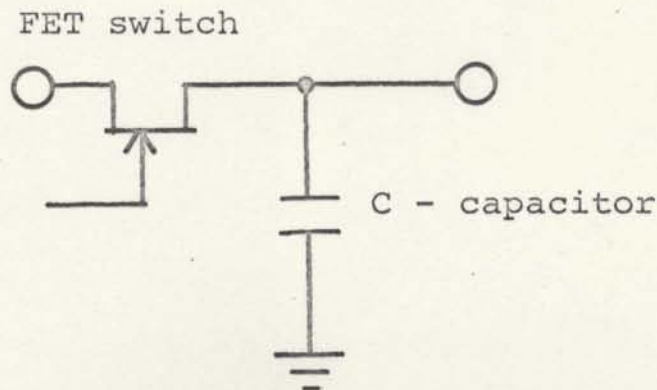


Figure I-2. Common S&H Circuit

The utilization of real world components introduces some complications. The electronic field effect transistor (FET) switch has finite ON (in the sample condition) and OFF (in the hold condition) resistances associated with it and a reaction time (time to turn ON/OFF once a command signal is received). Also, the capacitor memory device has a leakage current (loss of signal while in hold condition) and an acquisition time (time it takes for the capacitor memory device to fully charge up to - or sample - the signal level) associated with it. The reaction time of the electronic FET switch causes an error in the hold signal known as aperture error and the ON resistance of the

FET causes the capacitor memory device to take a finite time to charge up to the signal level. If the frequency components of the signal are too high, or the sample period too short, excessive errors may result. The capacitor leakage and the finite OFF resistance of the FET cause the memorized (held) signal value to droop or fall off with time. Figure I-3 exhibits these problems graphically.

Since we are considering the real world, we should note that the signal source will also have some impedance associated with it and must be added to the FET's ON resistance when computing the acquisition time of the capacitor. Also, the place(s) to which the output signal goes will have a finite input resistance and/or a bias current associated with it that will make the leakage (output signal droop) of signal more pronounced while in the hold mode.

Often the signal source impedance, the output load impedance, and the required bias currents will change as the signal level or other circuit conditions change. This causes the S&H output signal to be somewhat unpredictable. Several steps can be taken to minimize the effect of this unpredictability. A resistance that is very large with respect to the FET's ON resistance, plus the signal source impedance, is

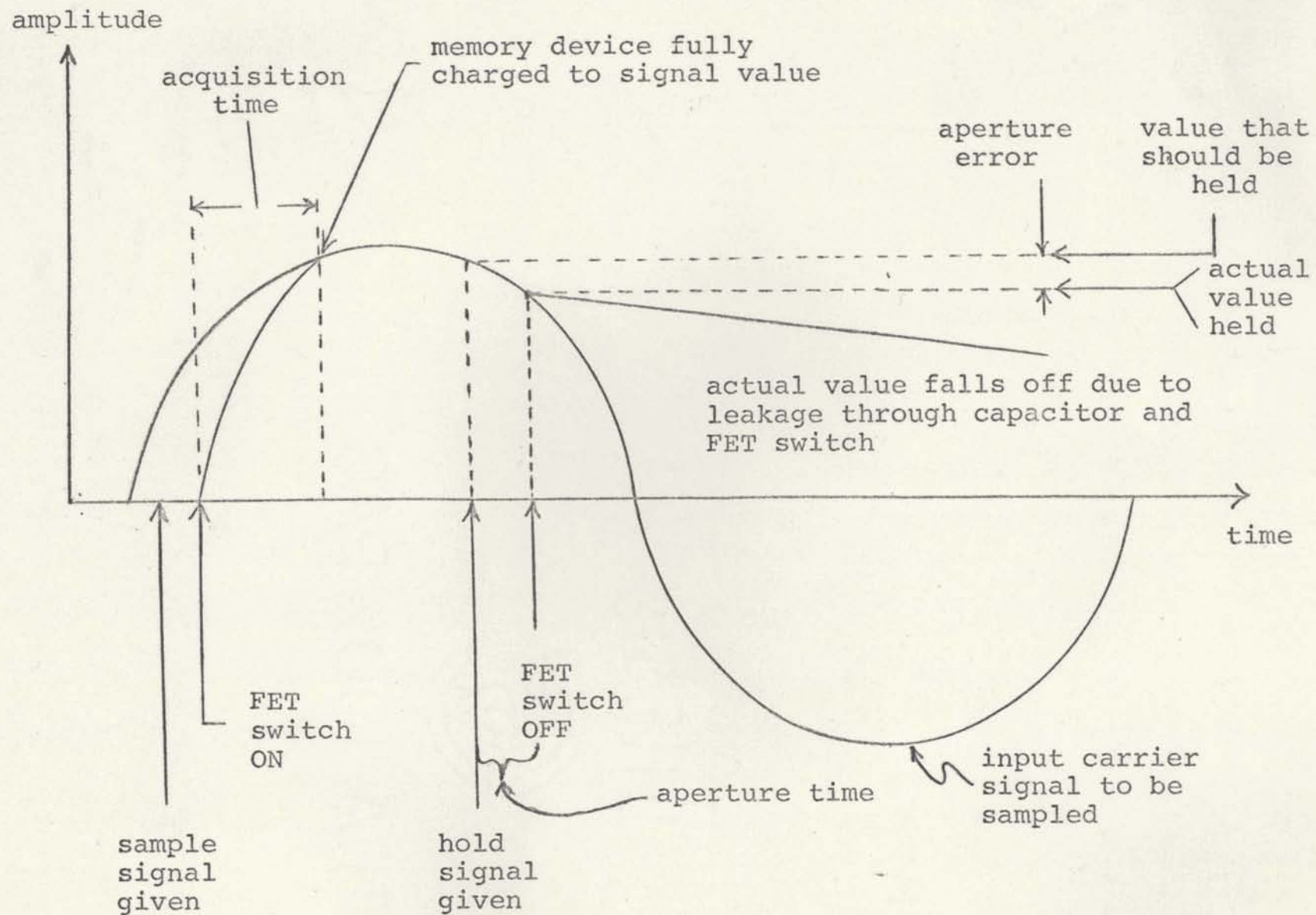


Figure I-3. Graphic Representation of S&H Errors

often placed in the input signal path, while on the output, a buffer amplifier with a known impedance and bias current is used as a load. This amplifier, in turn, outputs the S&H signal to the unpredictable loads. Figure I-4 shows the complete basic modern S&H circuit.

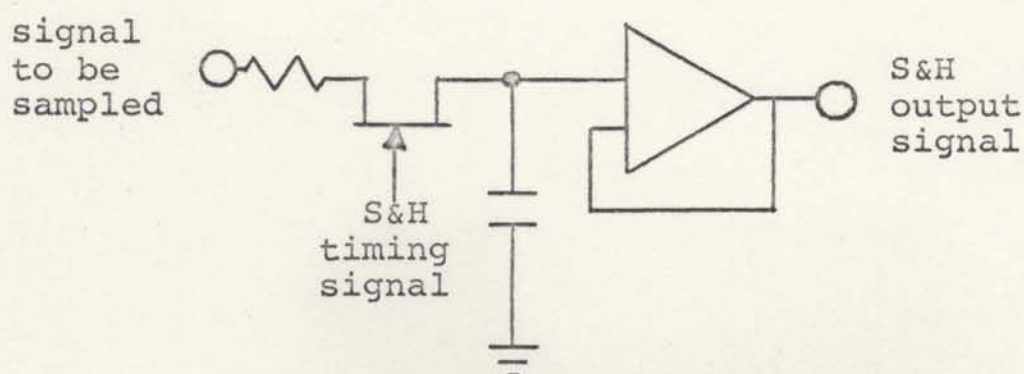


Figure I-4. Complete, Modern, Basic S&H Circuit

We have now improved the predictability of the circuit, but, have made the charging time of the capacitor longer:

$$t_{\text{CHARGE99\%}} = 4.605 \times C \times (R_{\text{ADDED}} + R_{\text{SOURCE}} + R_{\text{FET ON}})$$

$$t_{\text{CHARGE99.9\%}} = 6.91 \times C \times (\text{combined } R\text{'s}).$$

The droop of the S&H output is now

$$V_{\text{OUT}} = V_{\text{ORIGINAL}} \times \exp\left(-\frac{t}{R_T C}\right) - \frac{1}{C} \int_0^t i_{\text{CL}} dt$$

where R_T is the parallel combination of $R_{\text{FET OFF}}$ with $R_{\text{AMPLIFIER INPUT}}$ and, i_{CL} is the capacitor leakage current plus the amplifier bias current (we have assumed

that the amplifier gain is unity).

Typical values of $R_{FET\ ON}$ are 30Ω to 200Ω while typical values of $R_{FET\ OFF}$ are $10^8\Omega$ to $10^{13}\Omega$. This indicates that a typical added in resistor should be 300Ω to $2K\Omega$ just to make the $R_{FET\ ON}$ insignificant (signal source impedances vary considerably and will also add to the necessary value of R_{ADDED}). From the above we can see that the choice of C must be large enough to keep the output droop acceptable but small enough to allow charging to an acceptable percentage of the desired value in the necessary time.

Several variations of our modern basic sample and hold circuit are often used. One of these uses the capacitance as a feedback element (Figure I-5a). This has the advantage that the S&H can have gain (R_F/R_N) but, the S&H output is the inverse of the signal sample. Figure I-5b shows a variation that all but eliminates the effects of bias currents on output droop in the hold mode. In this design only offset currents (the difference between the inverting and non-inverting input bias currents) can affect droop. Figure I-5c shows a scheme¹ for making the acquisition time very short by adding a high capacitor charging current capability.

¹James K. Roberge, Operational Amplifiers Theory and Practice, (New York: John Wiley & Sons, Inc., 1975), p. 457.

Many unusual circuits have been designed to accomplish special tasks - one of these is shown in Figure I-6. It is an S&H with no droop (infinite holding capability) that uses an analog to digital conversion circuit with a digital to analog circuit in the feedback loop as the memory device. This design was disclosed by Burr Brown Corp. during a seminar on their conversion products held at Martin Marietta Aerospace in Orlando, Florida on September 17, 1975.

Using the theory and techniques presented in this chapter, a real signal processing problem was solved by designing an original, differential sample and hold circuit. The problem alluded to is presented in Chapter II and the circuit design is presented in Chapter III.

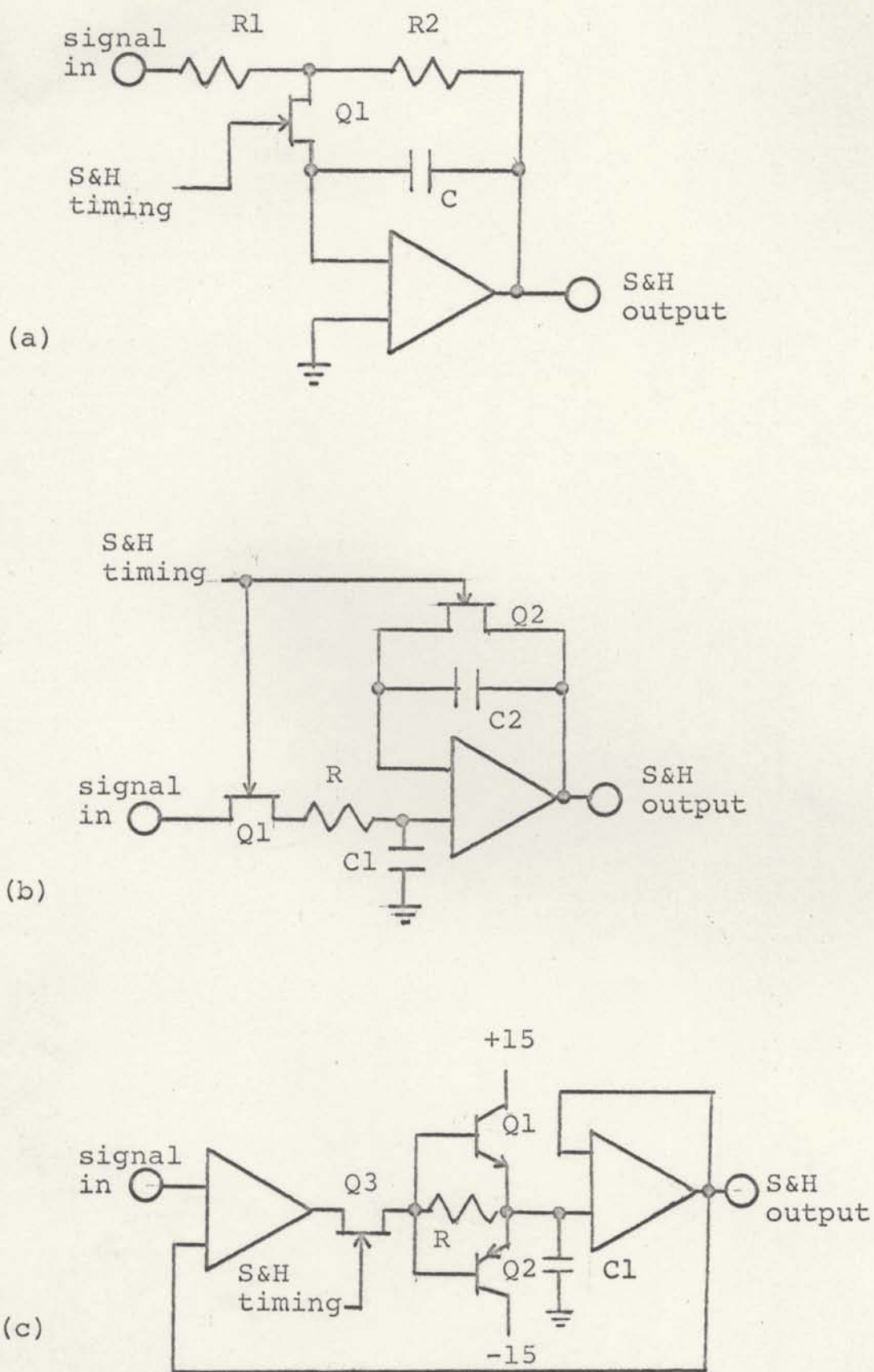


Figure I-5. Showing Some Variations of Modern S&H Circuits

ADC80 APPLICATION

(used with the permission of Burr Brown Research Corporation)

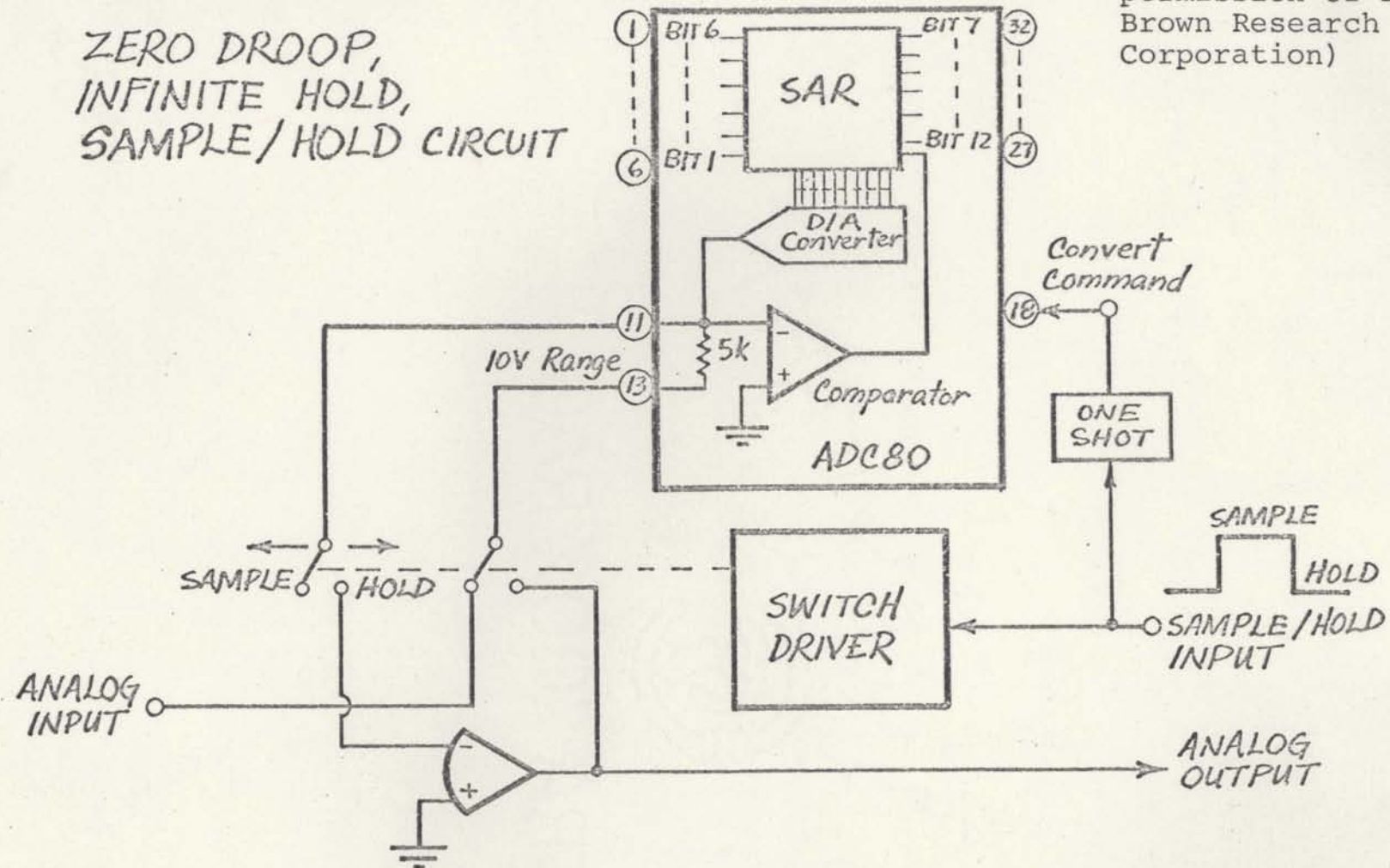


Figure I-6. A zero droop, infinite hold S&H circuit

CHAPTER II

THE PROBLEM TO BE SOLVED

In a system that requires an analog to digital interface, three amplitude modulated direction cosine signals representing angular target-location information and a reference signal are to be synchronously demodulated in an unusual noise environment, and presented to analog to digital (A/D) conversion circuitry with a very high degree of accuracy.

The System

The system is an airborne fire control system that searches for (scans ground areas in front of the aircraft), identifies, "locks on", and tracks ground targets. The target's angular location with respect to the aircraft (airframe) co-ordinates is transformed and the information is presented to an on board digital computer. This computer in turn generates steering commands, and computes optimum weapon release/fire times for the selected ordnance. This, of course, facilitates very accurate, automatic airborne-tactical-weapons delivery.

The system consists of three major sub-systems: the on board computer, the search and tracking unit (a pod mounted under the aircraft), and an aircraft interface unit (AIU). The AIU's purpose is to interface the pod's analog circuitry with the aircraft's digital computer.

In operation the pod (tracking unit) detects coded light pulses reflecting from a target (the light is actually coded pulses of laser light that is focused onto the target by a ground observer or another forward-air-control aircraft) and decodes it for identification purposes. If it is the proper code the "lock on" will occur and the light detector apparatus (gimbal mounted in the pod) will remain pointed directly (track) at the target. Then, gimbal position information that precisely defines the target line of sight co-ordinates is output as electronic analog signals.

The AIU transforms the electronic analog signals from the pod to digital ones with a format acceptable to the on board computer. This is where our problem exists as will be discussed later in detail.

The manner in which the computer interprets the three direction cosine signals is of great importance, since it will materially affect our design problem. The azimuth and elevation angles are the ones used for

steering and weapons release commands and are computed as follows:

$$\text{azimuth} = \text{Arctan } \frac{Y}{X}$$

$$\text{elevation} = \text{Arctan } \frac{Z}{\sqrt{X^2 + Y^2}}$$

As this indicates, scale factor (gain) errors are meaningless when the scale factor errors are identical to each other in all three (X, Y & Z) direction cosine signals, i.e.

$$\text{Arctan } \frac{KZ}{\sqrt{(KX)^2 + (KY)^2}} = \text{Arctan } \frac{Z}{\sqrt{X^2 + Y^2}}$$

This will serve to relax the design criteria such that we can allow identical scale factor errors on all signals simultaneously. We will term this condition scale factor error equivalence cancellation and will abbreviate it SFEEC.

The Interface Subsystem

The aircraft interface unit converts the analog direction cosine signals to a format acceptable to the digital computer. This is accomplished by synchronously demodulating the three direction cosine signals (resolver outputs) and a reference signal (the resolvers excitation voltage) then doing a classical analog to digital (A/D) conversion on the resultant demodulated voltage levels. The A/D conversions are done by one A/D con-

version circuit in a time multiplex fashion. This A/D circuit accepts the demodulated reference voltage such that the resultant digital output representation will be

$$\frac{\text{input signal amplitude}}{\text{reference amplitude}}$$

Thus, a full scale positive (input = reference) signal results in a positive full scale output (+1) representation, and a full scale negative (input = -reference) results in a negative full scale output (-1), while no input (input = 0.0V) results in a zero output (0) representation.

The Error Budget

The interface subsystem must meet a rather tight error specification. The input to output, one sigma, error allowed is 1.5 milliradians (mr) of spherical pointing vector error. The one sigma specification means that 68.268% of the data points to be transmitted in all of the units we will manufacture must not have greater than this error. In other words, we must be able to show mathematically that our design will, in general, meet the 1.5 mr requirement. However, since we must be content to test only a single trial unit before production begins on the units to be delivered, we may accept absolute maximum three sigma (4.5 mr)

error measurements, as long as the average measured error is still within one sigma limits.

This 1.5 mr error specification has meaning in voltage only if the pointing vector has been precisely specified. However, for the case where the errors are similar - but opposite in sign - in all three direction cosines (our most common case), the vector defined by 45° azimuth and 45° elevation is a worst case condition. We must, therefore, determine the voltage error equivalent of 1.5 mr at 45° azimuth and 45° elevation.

Now, 1.5 mr of spatial error is equivalent to 1.0607 mr of worst case planar angle error. We can, therefore, conservatively allow 1.06 mr of error in azimuth and/or elevation. Or, to be more specific, we will allow errors in the digital representation equivalent to 0.060733 degrees at 45° (45.060733° and 44.939267°). From this we can easily compute that the equivalent percentage errors for the X and Y signals are 0.212%. But only 0.106% for the Z direction cosine signal. Since our system is based on 10V ($\sin 90^\circ = 10V$) this is equivalent to a 7.5 mV (at 45°) error in the Z direction cosine signal. Because any error introduced into one signal is likely to be introduced into any (or both) of the other signals, conservative design practice dictates that our error budget allow no more than 7.5 mV

equivalent error on any signal from input to output. This must be the maximum statistically predictable error due to all causes.

Since non-related and independent error sources may tend to be additive or cancel, the predicted error due to n of these sources will be

$$\sqrt{(\text{error \# 1})^2 + (\text{error \# 2})^2 + \dots + (\text{error \# n})^2}.$$

This is the root of the sum of the squares (RSS) of the possible errors. It is the way that all of the predicted errors in the whole system are computed (a contractual requirement).

The A/D converter has a specified maximum error of plus or minus one least significant bit (LSB). It is a 12 bit A/D with one bit being used as a sign bit. Thus, one LSB is equivalent to

$$\frac{\text{full scale}}{2^{11}} = \frac{\text{full scale}}{2048} = 4.88 \times 10^{-4} \times \text{full scale}$$

This indicates that the maximum error introduced by the A/D will be 0.000488 times full scale. Now, in this system 10 volts is full scale. Therefore, the error budget for the remaining demodulator (S&H) portion will have to be $\sqrt{(7.5 \times 10^{-3})^2 - (4.88 \times 10^{-3})^2}$ or 5.695mv. This is 0.0739% of our critical voltage ($10 \sin 45^\circ = 7.071V$) and is the maximum allowable demodulator error due to all sources (keep in mind that error here

means only scale factor differences or inequalities between the signals - not absolute magnitude errors). Note that this must also take into account the end of life (3 years) tolerance on all the components.

The A/D reference signal is to be derived from the reference signal such that any error in this derivation shall be translated into scale factor error and shall be caused to be equal in magnitude and sign to like errors imposed on all three of the direction cosine signals. This will allow accurate scale factor conversion since the reference scale factor error will be (by definition) equal to the signal scale factor errors. The A/D output will then be

$$\frac{\text{signal}}{\text{reference}} \times \frac{(\text{scale factor error})}{(\text{scale factor error})}$$

which is equivalent to

$$\frac{\text{signal with no error}}{\text{reference with no error}}$$

since the scale factor errors are exactly equal.

It is, therefore, our responsibility to make it so; anything less than this must be considered as a source of error.

The Input Signals

Three analog direction cosine signals (X, Y & Z) containing target (gimbal) line of sight information are

present at the output of the pod. These signals are 10V peak, 1800Hz, sinusoidal, amplitude modulated resolver outputs. The resolver excitation voltage is also supplied as a reference (REF) such that positive and negative signals may be defined as indicated in Figure II-1.

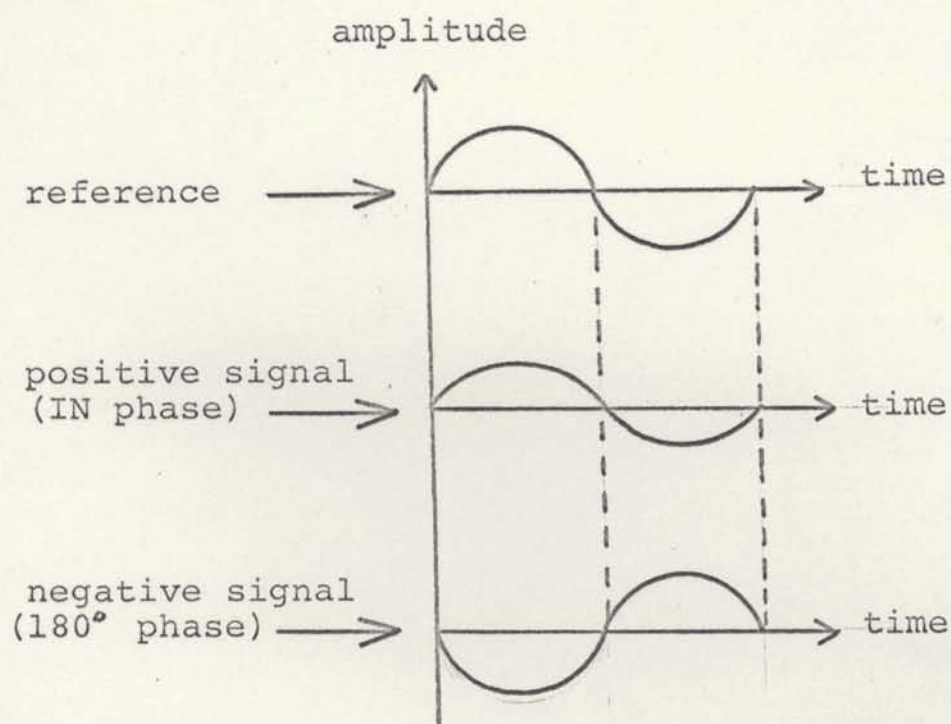


Figure II-1. Indicating How Sign Is Defined

It will be necessary to make the positive/negative determination and cause a sign bit to be set or re-set in the digital word format to the computer that will represent the direction cosine signals.

The direction cosine signals and the reference signal are supplied on two lines, signal high and signal low (signal low is a central ground point in

the pod). These signals are to be differentially received with at least 10K ohms differential impedance, 10K ohms impedance to ground, and no more than 20pF of capacitance to ground.

Electrical power is also supplied on three lines:

1. $5v \pm 1\%$, 2% ripple (p-p), 0.5 amperes
2. $15v \pm 0.5\%$, 1% ripple (p-p), 0.2 amperes
3. $15v \pm 0.5\%$, 1% ripple (p-p), 0.2 amperes

The Synchronous Demodulator - Our Design Problem

One attempt to implement the necessary synchronous demodulation of the signals has been only semi-successfully accomplished. The essence of that design is as shown in Figure II-2. This is included here because part of our task will be to utilize as much existing circuitry as possible in order to minimize the number of added parts and also to standardize parts.

There was an unforeseen problem that kept the first design from being entirely successful. A pulse of current is intermittently coupled into the 1800Hz signal (but not the reference) lines from nearby torque motor power control lines. This pulse is of sufficient amplitude to result in a 1V maximum offset shift in the average or DC value of the direction cosine signals. Also, the amount of offset shift is

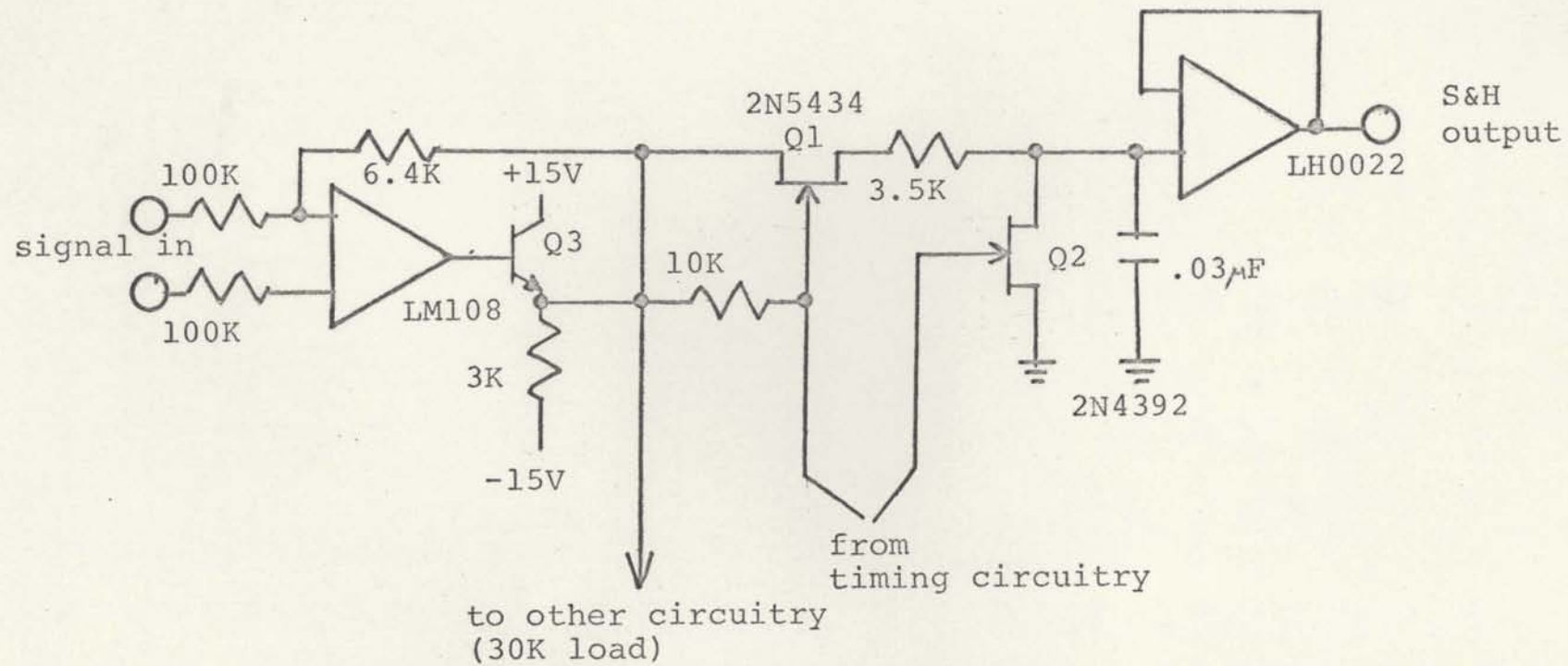


Figure II-2. The Old Design

not the same for all three signals nor does it have anything to do with the magnitude of any of the signals. Therefore, we cannot count on scale factor equivalence cancellation (SFEEC) to help us out here. The duration of the offset shift varies from approximately one to five cycles of the 1800Hz signals. This "noise" signal, therefore, can be neither filtered nor blocked out. The first design could not reject this "noise" because each sample of the direction cosine signals included the noise offsets and there was no subsequent way to subtract them out of the samples.

Our task, then, is to design a set of circuits that will synchronously demodulate three, 10V peak, 1800Hz, amplitude modulated, sine wave, direction cosine signals having as much as 1V of DC offset and that will present accurately scaled representations of these signals along with a similarly scaled representation of an 1800Hz reference signal to an analog to digital conversion circuit. These circuits may not introduce errors such that any one signal shall vary more than 0.075% of full scale (7.5mV), one sigma, from absolutely accurate. However, scale factor errors, of any magnitude, such that

$$X_{OUT} = (SF)(X_{IN})$$

$$Y_{OUT} = (SF) (Y_{IN})$$

$$Z_{OUT} = (SF) (Z_{IN})$$

$$REF_{OUT} = (SF) (REF_{IN})$$

where SF is equal in all three, may be allowed. Scale factor differences, from one direction cosine signal to the next, must be treated as all other errors. In other words, the resulting output voltage error due to unequal scale factors must be considered just like the errors from all other sources when determining the total input to output signal error in any one signal.

CHAPTER III

THE CIRCUIT DESIGN

This chapter presents an original design solution to the problem discussed in Chapter II. It also includes the results of a breadboard test of the noise rejection scheme concept used.

In order to accomplish the design task (and the circuit rework) as simply as possible, with the fewest added parts and with no unnecessary conceptual changes, the new design will be, as much as possible, an extension of the old one. This means that the demodulation technique will remain the same, i.e. sample and hold. This will result in the fewest added part types. Also, most of the necessary timing signals are already present in the existing interface subsystem design. This will also automatically take care of the positive/negative sign determination in the A/D circuitry.

The Noise Rejection Scheme

Several schemes for synchronous demodulation exist that will reject 1.5V offsets, however, a literature search revealed none that were S&H circuits. Therefore,

in order to meet our requirements, an original method was devised. This new scheme involves sampling twice on the same cycle (at positive and negative values), then determining the difference between the two samples (being careful to observe signal polarity) and multiplying the result by an appropriate scale factor as follows:

$$X_{OUT} = \frac{X_{IN} \sin 120^\circ + \text{OFFSET} - (X_{IN} \sin 240^\circ + \text{OFFSET})}{2 \sin 60^\circ}$$

$$X_{OUT} = X_{IN} \frac{\sin 120^\circ - \sin 240^\circ}{2 \sin 60^\circ} = X_{IN}$$

The 120° and 240° sample points were chosen to eliminate possible problems with third harmonic distortion (a common problem in resolver outputs). This is represented graphically in Figure III-1.

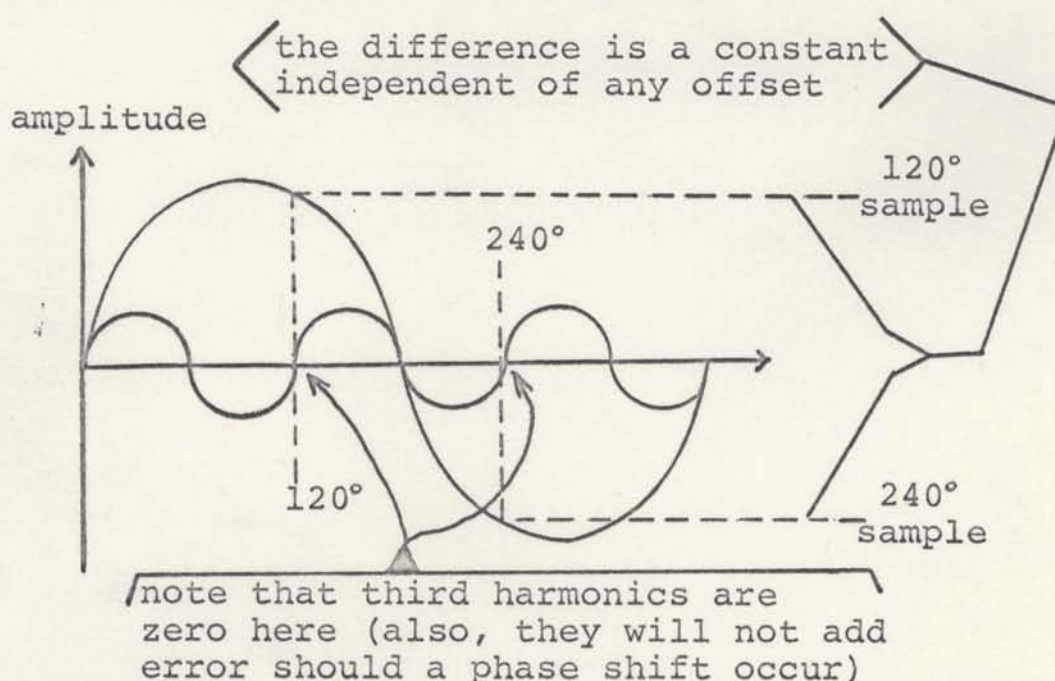
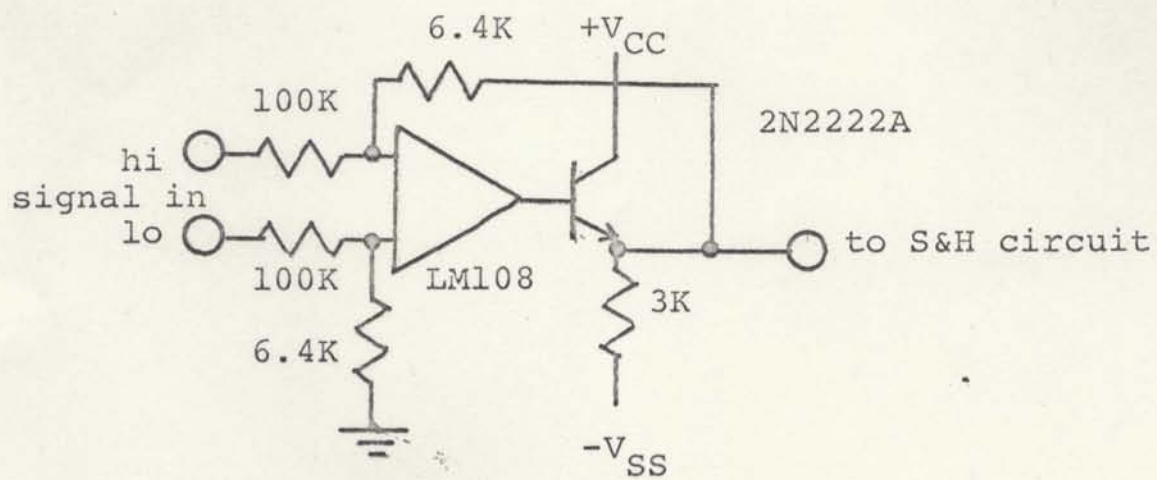


Figure III-1. Graphic Representation of Scheme To Reject Offset Conditions

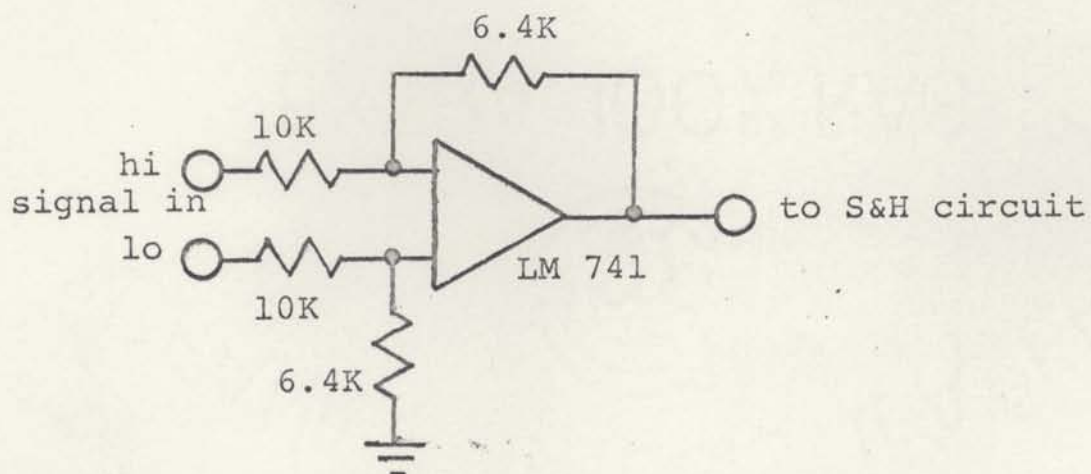
The Input Stage

The input stage of the original design could be retained exactly as it is (Figure III-2a) since its output goes to other circuitry besides ours and it could easily meet our requirements. However, the LM108 op amp used here is expensive and the 2N2222A transistor is necessary only because of the LM108's limited output current capacity. This original circuit was designed to have a minimum offset with very large (100k) input impedance characteristics - neither of which is now necessary (the signal source characteristics have changed). We will, therefore, use a 741 op amp (already used in the subsystem) with reduced input and feedback resistor values but keep the same (0.64) first stage gain. (See Figure III-2b).

In order to avoid non-linearities our maximum signal amplitude (including the expected offsets) should not exceed 10V. The input buffer stage in the existing design has a gain of 0.64 which will leave room for a 3.6V offset if necessary. Since changing the gain of this stage would also create a requirement to make changes in the A/D circuit, it will remain the same.



(a)



(b)

Figure III-2. The Input Stage
(a) Old, (b) New

This circuit configuration is capable of adding several millivolts of offset error, however, since this kind of error is exactly what the new S&H circuitry will be designed to eliminate or reject, this should not impact the error budget at all. It can be shown¹ that this offset will be roughly 8mv maximum. Also, this offset will not cause any problems in the other circuitry to which the output goes. In addition, since the common mode rejection ratio is 70dB (min) and the large signal voltage gain is 87dB (min), any non-linearities or common mode problems should be negligible.

The input and the feedback resistors have a tolerance of 0.005% with 50ppm end of life tolerance and $\frac{1}{2}$ ppm/°C tracking over temperature² (absolute is not important here since we are working with ratios). The tracking over time is 22ppm (again absolute is not important). Assuming all of these to be additive, the total resistor tolerance over temperature and end of life is 0.0125%. From this, we can calculate that

¹Linear Integrated Circuits (Santa Clara, California: National Semiconductor Corporation, 1975), pp. 2-229 and 2-230.

²Precision Resistors. Catalog. (Malvern, Pennsylvania: Vishay Resistive Systems Group, n.d.).

the maximum possible gain error in the first stage is

$$\frac{6.4K (1 + .000125)}{10.0K (1 - .000125)} = .64016$$

$$\frac{0.64016}{0.64} = 1.00025 \text{ or } 0.025\% \text{ error}$$

The Sample and Hold Stage

The old S&H circuit schematic is shown in Figure III-3 and the new S&H circuit schematic is shown in Figure III-4. The new circuit will accomplish the necessary differential arithmetic operation in that the output voltage will be the voltage at B' (sin 120°) minus the voltage at A' (sin 240°) multiplied by the gain, $1/(2 \sin 60^\circ)$. From these schematics, it may be seen that very few parts and only one new part type (LH0052) have been added. Several of the resistor and capacitor values have changed but the same part types are already in use in the subsystem. We could have just doubled the old design and added a differential amplifier but this would have resulted in too many parts, too much PC board "real estate" being used, and too much cost.

The existing timing signals from the old design will be utilized in so far as possible. These signals are illustrated in a timing diagram in Figure III-5. The last signal in this timing diagram will be generated by new circuitry. The new (added) timing signal is generated from a single monostable multivibrator (5N54121W)

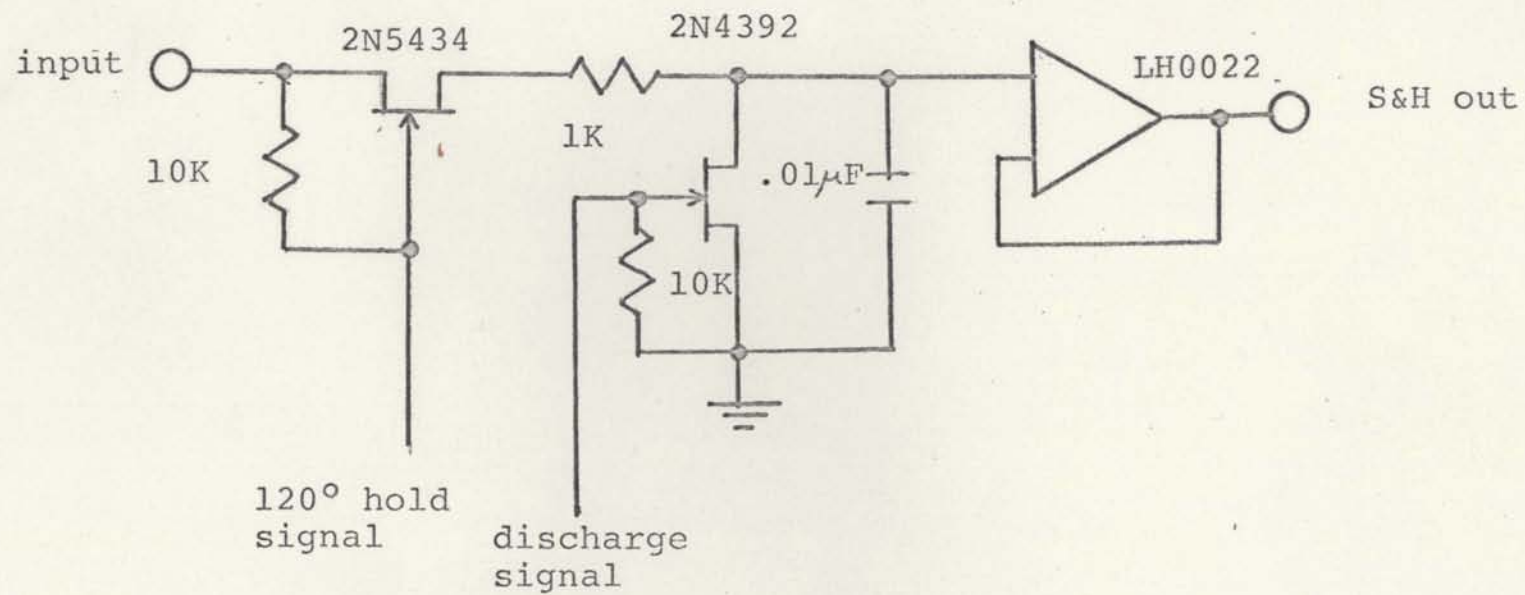


Figure III-3. The Old Design

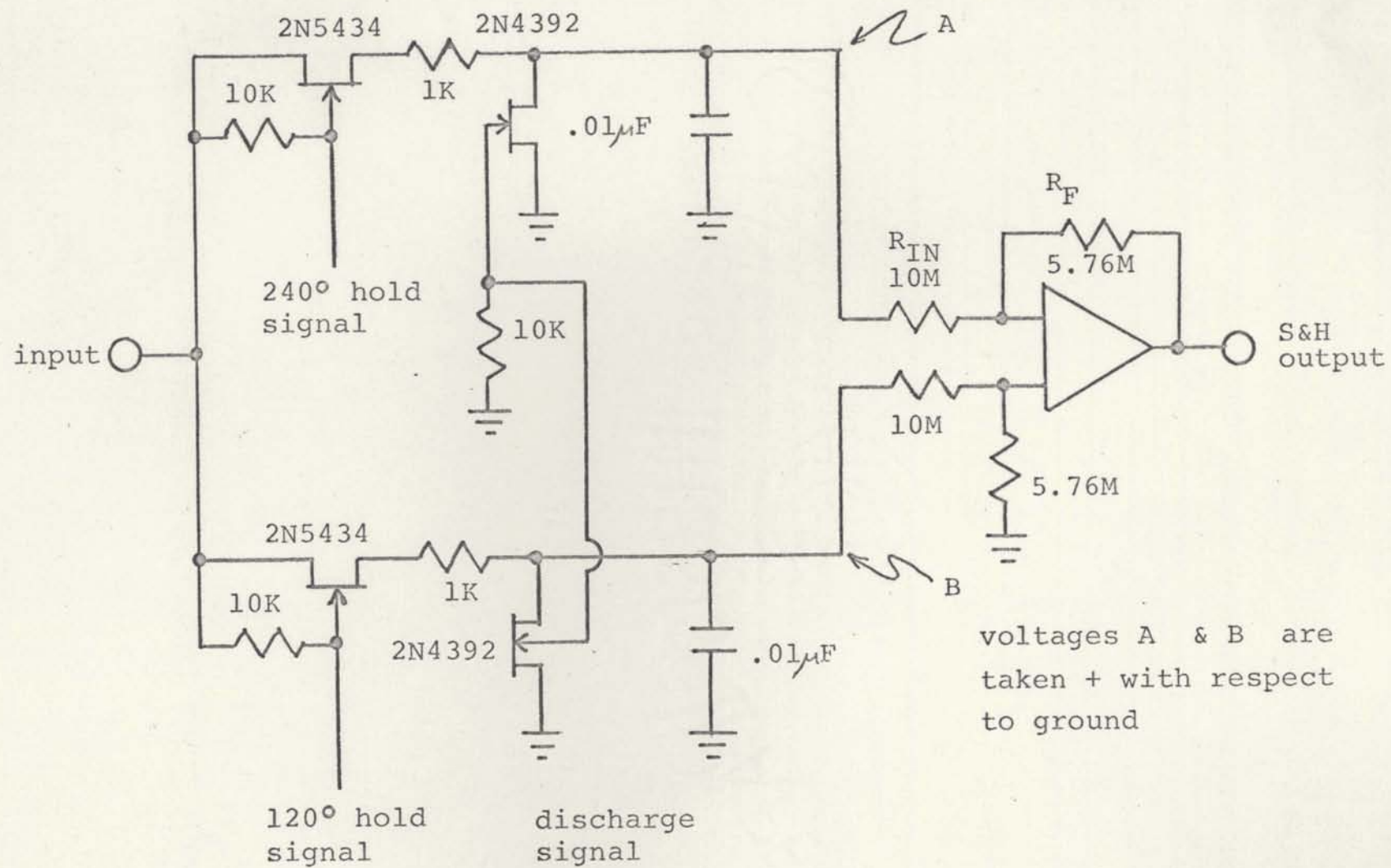


Figure III-4. The New Design

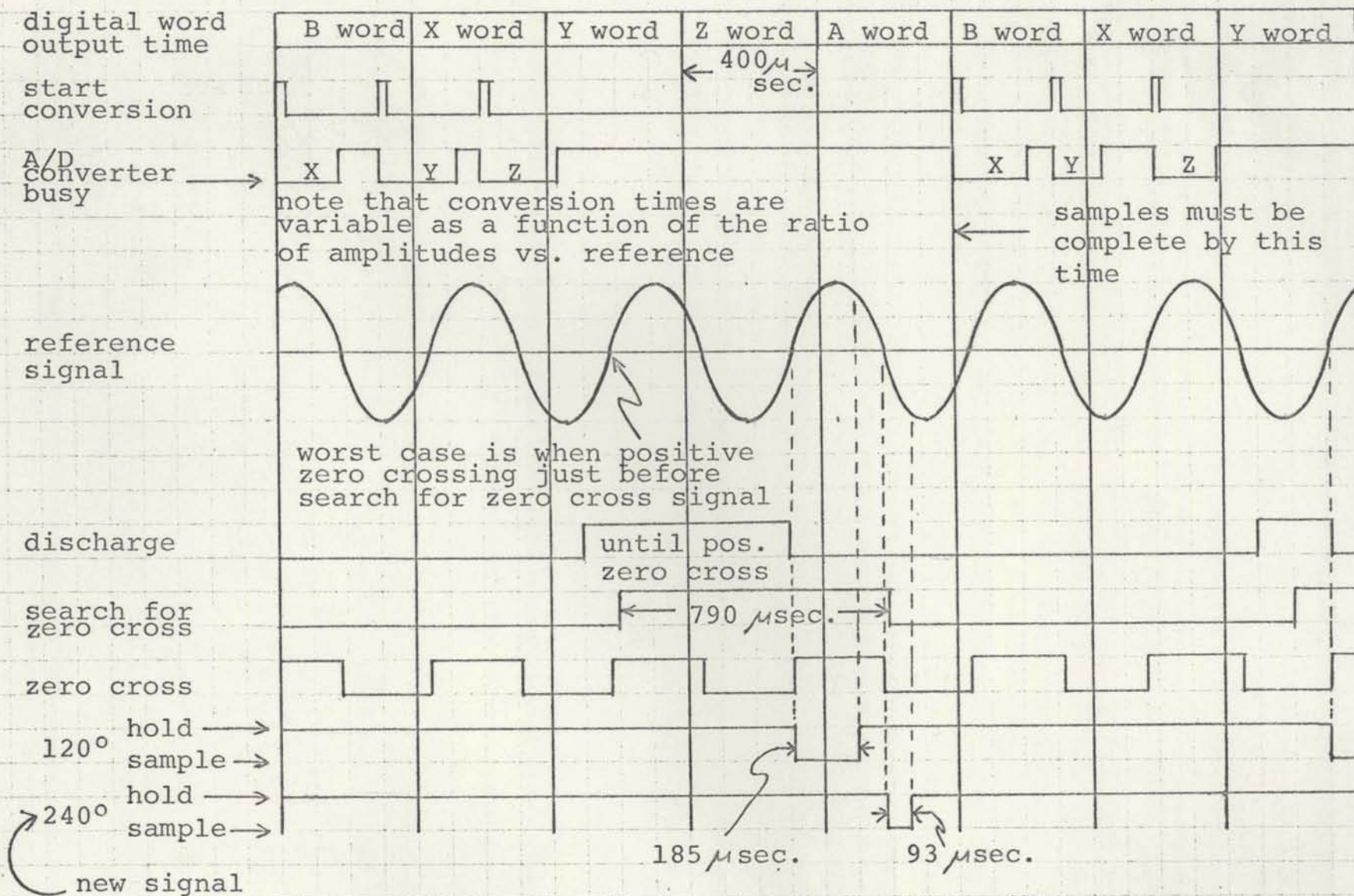


Figure III-5. The Timing Signals -- Old and New

as shown¹ in Figure III-6. Note that a new (already in use in the subsystem elsewhere) FET switch driver circuit, siliconix D129² is also shown here. This new timing signal is to control the sample and hold times of the 240° sample. It is designed to cause the 240° sample to begin sampling at the first negative zero crossing after the 120° hold has begun, and, to sample for 93 microsec.¹ (approximately 60°), then, to hold until another 120° sample has been taken. (The end of the discharge capacitor signal is derived from the 120° sample signal and occurs approximately 35 microsec. later than the zero crossing signal; thus a mis-trigger situation is avoided). The exact timing of this signal is not critical since any error here creates equal scale factor errors in all channels (SFEEC again). The output stage of this design will multiply the difference between the 120° sample and the 240° sample by the appropriate scale factor - $1/(2\sin 60^\circ)$ - to make the output voltage represent 10V (actually 10V peak). To determine the ratio of the output stage feedback resistor to the non-inverting input resistor we calculate as follows: (see Figure III-3b).

¹Integrated Circuits Catalog for Design Engineers (Dallas, Texas: Texas Instruments Inc., Components Group, n.d.), pp. 6.72 - 6.78.

²Siliconix Inc., Siliconix Integrated Circuits Data-book (Santa Clara, California: Siliconix Inc. 1975), pp. 2.5-6.

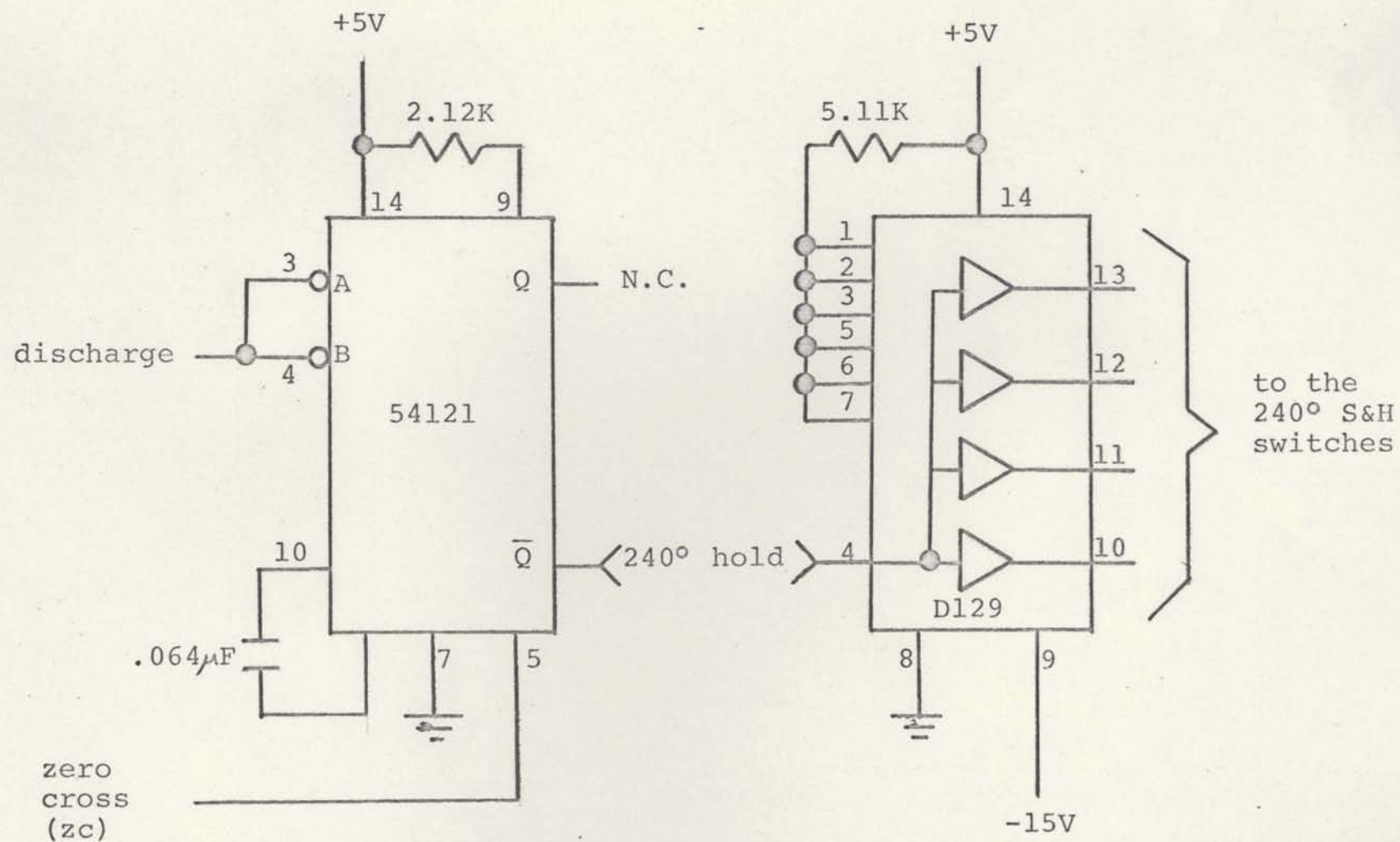


Figure III-6. New Timing Circuitry

$$\text{point A} = 6.4 \times \sin 240^\circ = -5.54256\text{V}$$

$$\text{point B} = 6.4 \times \sin 120^\circ = 5.54256\text{V}$$

$$\begin{aligned} V_{\text{OUT}} &= \left[B \times \frac{R_F}{R_{\text{IN}} + R_F} - A \right] \times \frac{R_F}{R_{\text{IN}}} + B \times \frac{R_F}{R_F + R_{\text{IN}}} \\ &= [B - A] \frac{R_F}{R_{\text{IN}}} \end{aligned}$$

but since V_{OUT} must = 6.4V

$$R_F = \frac{6.4 R_{\text{IN}}}{B - A} = 0.57735 R_{\text{IN}}$$

we will use the nearest standard decade resistor value, 0.576. Later we will see that this is permissible.

We must now consider the voltage droop on the holding capacitors over the maximum time period between the earliest possible sample time and the last A/D conversion (1.9×10^{-3} seconds maximum - see Figure III-5). In order to do this for a worst case analysis, we will treat the op amp non-inverting input node voltage (0.576 the 120° hold voltage) as a step forcing function (this is worse than the worst case the circuit can see in operation). The 240° capacitor hold voltage is then

$$V_{\text{IN}} \sin 240^\circ [1.576 \exp(-t/RC) - 0.576]$$

and the 120° capacitor hold voltage is

$$V_{\text{IN}} \sin 120^\circ [\exp(-t/RC)]$$

If we assume full scale input voltages are to be held on the capacitors we can calculate the voltages remaining on the capacitors after 1.5 microsec. with various

values of resistance in the input paths to the op amp. A 10K ohm resistor results in a 240° capacitor voltage of +3.143 volts that ideally should be -5.54256V. This of course, will never do. An increase in resistance to 100K ohms results in a hold voltage of +1.886 volts - still not enough. Another decade increase to 1M ohm results in -4.031 volts or a 27% error. Another increase to 10M ohms results in -5.41251 volts being held after 1.9microsec. This is an error of 2.966%.

Now the voltage remaining on the 120° holding capacitor using 10M resistors is +5.46004v. This is an error of 1.8821%. Together these errors result in a differential output error from the S&H circuit of 2.424% (6.2302464v versus the ideal of 6.3850291v). This still seems to be unacceptable to the casual observer. However, we know that errors of equal scale factor magnitudes and signs on all the signals will not be interpreted as errors by the system. Since the percent of error generated is always the same no matter what the signal amplitude or sign may be, SFEEC will occur:

$$\begin{aligned}
 V_{OUT} &= \frac{1}{C} \int_0^T \frac{V_{IN} \sin 120^\circ - V_{IN} \sin 240^\circ}{R_{INPUT}} dt \\
 &= V_{IN} \frac{1}{C} \int_0^T \frac{\sin 120^\circ - \sin 240^\circ}{R_{INPUT}} dt
 \end{aligned}$$

$$V_{OUT} = V_{IN} \times \text{constant}$$

thus,

$$\frac{V_{OUT}}{V'_{OUT}} = \frac{V_{IN} \times \text{constant}}{V'_{IN} \times \text{constant}} = \frac{V_{IN}}{V'_{IN}}$$

Therefore, any droop in hold voltage due to this cause is not a source of error. Also, since the A/D reference voltage is processed exactly the same way, we don't even need to change the output stage gain (from this we see that standard resistor values can be used without adverse effects). However, a difference in droop from one signal channel to another can occur here with changes in time-constant due to differences in hold capacitance and/or the resistor in the inverting input line to the op amp. The maximum possible error here, assuming the resistor and capacitors of one channel to be maximum while another channel is minimum, is 0.00247%, which is small but not negligible.

We cannot obtain the 0.005% Vishay resistors in these high ohmic values. We can, however, safely assume that resistors with these values can be procured at less than twice the tolerance of those we used in the first stage. We can have, therefore, a gain error of as much as 0.05%.

If we consider the effects of the op amp bias currents on droop, we find that only the differences

in bias currents between the inverting and non-inverting inputs (offset bias currents) can cause error. To see this, we must realize that bias currents are either all into the amplifier or all out of the amplifier (not both) on both inputs. This either raises or lowers the voltage held on the capacitors equally:

$$\frac{dv_C(t)}{dt} = \frac{1}{C} \frac{dq(t)}{dt} = \frac{i(t)}{C}$$

Thus, the difference between the two remains the same no matter how large the bias currents happen to be. In our case, the LH0052 has a maximum offset bias current (over temperature and time) of 152×10^{-12} amps. Therefore, we can calculate the maximum difference between X, Y and Z signal outputs due to offset bias currents to be 0.572mV. At 45° equivalent voltage levels, this turns out to be a 0.013% error.

Now the variations in output voltage due to the op amps internal offsets are, according to the LH0052 specification¹, 1.3mV over temperature and time. This results in an error (at 45°) of 0.028%.

¹Linear Integrated Circuits (Santa Clara, California: National Semiconductor Corporation, 1975), pp. 2.29 - 2.35.

In considering the capacitor voltage droop due to capacitor leakage and the reverse bias leakage of the FET switches, we see that once again only the differences in leakage between channels and between the 240° side and the 120° side of any single channel can result in errors. We will, therefore, assume that the differences in leakage in the capacitors to be $\frac{1}{4}$ of the maximum leakage (40×10^{12} amperes) and the leakage in the FET switches to be $\frac{1}{4}$ of the maximum leakage (0.2×10^{-9} amp). At 45° equivalent voltage levels, this results in capacitor voltage changes of:

$$\begin{aligned}\Delta e(t) &= \frac{1}{C} \int_0^t i_L dt \\ \Delta E &= \frac{10^6}{0.01} \int_0^{1.9 \times 10^{-3}} 0.24 \times 10^{-9} dt \\ &= 0.046 \text{ mV}\end{aligned}$$

where i_L represents the combined leakage current components. This represents an output error of 0.001% at 45° equivalent voltage levels.

Another error we can have is an error that comes from different acquisition time time-constants due to variations in resistor (0.01%) and capacitor (0.1%) tolerances¹. Using

¹Telephone interview with Dave Kellerman, Component Research Corporation, Los Angeles, California, 12 September 1975.

$$v_C(t) = V_{IN} [1 - \exp(-t/RC)]$$

it can be shown that the maximum voltage error here is $3 \times 10^{-9}V$ or 0.00000074% (this is negligible).

Aperture error can occur here if one of the FET switches is slower to turn off than the other FET switches in the system. The maximum turn off time of a 2N5434 FET is 36×10^{-9} seconds¹. Some tracking must occur, so we will assume a "slowness" of $\frac{1}{2}$ speed (18×10^{-9} seconds) for one FET. This results in 0.0059% (0.266mV) output error at 45° equivalent voltage levels.

The Error Total

All of the errors are shown in Table III-1.

ERROR SOURCE	ERROR
First Stage	0.025%
S&H Stage	
Output Gain	0.050%
Hold Droop	0.002%
Offset Bias Current	0.013%
Offset Voltage	0.028%
Capacitor/FET Leakage	0.001%
Aperture Error	0.006%

Table III-1. Indicating Computed Errors

¹Transistors. Catalog. (Santa Clara, California: National Semiconductor Corporation, 1975), p. 47.

As discussed in Chapter II, the total statistically predictable error due to independent error sources is the RSS of all the errors. Therefore, the maximum error we can predict in the new demodulator portion is

$$\sqrt{(0.025\%)^2 + (0.050\%)^2 + (0.002\%)^2 + (0.013\%)^2 + (0.028\%)^2 + (0.001\%)^2 + (0.006\%)^2}$$

or 0.064187%. Since the allowable error was 0.739% we find that we are well within a margin of safety. In addition, we have assumed many differences in device parameters from channel to channel that probably will never be as large as assumed. Even the resistor¹ and capacitor² values tend to track over temperature and end of life much more closely than indicated herein. Also, in at least one calculation, error sources have been treated as independent, where, they actually tended to cancel each other (i.e., the output stage gain and the hold droop). In order to increase our accuracies significantly, we could monitor and test (temperature cycle, reverse bias burn in, etc.) components to pick those that track best. Thus, this design is assured of meet-

¹Interview with Kurt Gonzenbach, Martin Marietta Aerospace, Orlando, Florida, 5 August 1975.

²Interview with Edward Hierholzer, Martin Marietta Aerospace, Orlando, Florida, 14 August 1975.

ing its contractual operational criteria.

The Breadboard Circuit

Building a complete system, even without an A/D converter, would be quite expensive. Also, the necessary parts are long lead time items since they have special characteristics (0.005% resistors, etc.). Therefore, testing of the circuitry and concepts in this research report will be limited to testing the concept of differential sampling to reject offset errors. It is felt that the worst case analysis for error sources is sufficient to show that the system can process the signals within the error budget without having to do a full scale pre-production breadboard test. To test the concept the circuit shown in Figure III-7 will be used.

In place of the very expensive LH0052 op amp and the high value resistors, buffer inverters (741's) are used to help reduce hold mode droop. Also, to facilitate testing and reduce the timing circuit complexity, the discharge FET switches are omitted.

In order to test the concept, offsets of 4.000V will be added to an 1800Hz sinusoidal waveform and the offsets measured at test points A and B and the S&H output. The test results are shown in Table III-2.

As can be seen from these test results, a plus or minus 4V offset in the signal results in only a

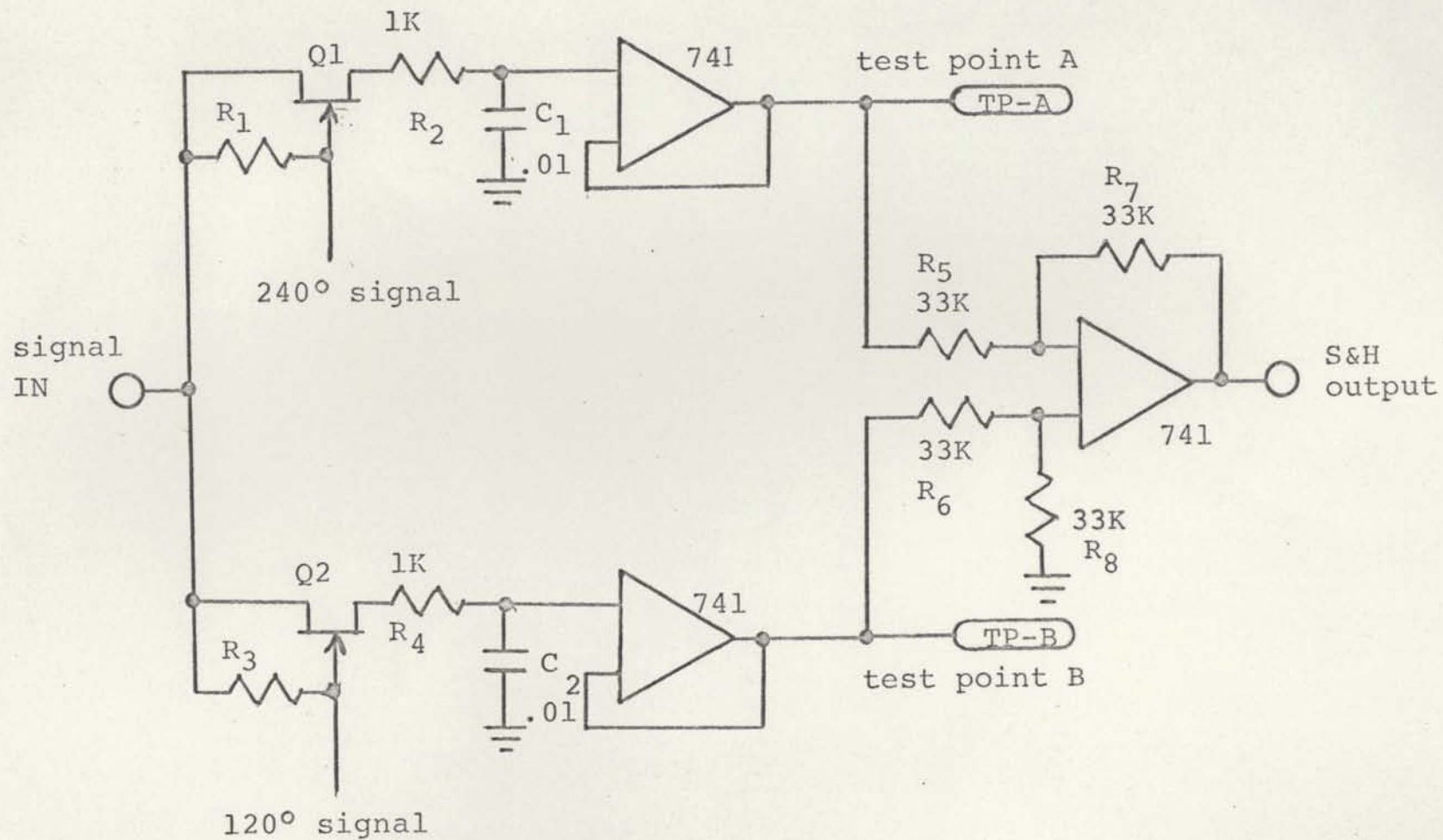


Figure III-7. The Breadboard Circuit

minus or plus (respectively) 4mV offset in the S&H output signal. This is a 60dB rejection ratio and is proof that the concept is a valid one.

OFFSETS			
INPUT	TP-A	TP-B	OUTPUT
0.000V	-17mV	+8mV	+23mV
-4.000V	-3.987V	-3.962V	+27mV
+4.000V	+3.952V	+3.976V	+19mV

Table III-2

CONCLUSIONS

The very careful (and conservative) worst case analysis in conjunction with the breadboard test results assures a technically feasible design. Our careful attention to minimizing added parts and part types, and the fact that no last minute adjustments or "tweakings" are required in this design assures a design well suited to high volume production. In short, this design will indeed perform the function for which it is intended. One word of caution is in order, however. In the event that a level change in the input offset voltage occurs between the 120° sample point and the 240° sample point during the particular waveform cycle being sampled, an error (equal to the step amplitude) would be passed through to the A/D

circuitry. This condition will not occur often and when it does it will result in no more error than would be present with the old design.

BIBLIOGRAPHY

- A High Speed Sample and Hold Using the μ A 715.
Application Brief 128. Mountain View,
California: Fairchild Semiconductor, 1969.
- Burlingame, B.G.; Kesner, D.; and Botos, R.A.
The Control Engineers Guide to IC Applica-
tions. Application Note 552. Phoenix,
Arizona: Motorola Semiconductor Products
Inc., 1971.
- English, M.J. An Improved Sample-and-Hold
Circuit Using the μ A740. Application Brief
165. Mountain View, California: Fairchild
Semiconductor, 1971.
- Field Effect Transistors in Chopper and Analog
Switching Circuits. Application Note 220.
Phoenix, Arizona: Motorola Semiconductor
Products, Inc., 1970.
- Frater, R.H. "Synchronous Integrator and Demodu-
lator". The Review of Scientific Instruments,
36 (May 1965): 634-637.
- Gonzenbach, Kurt. Martin Marietta Aerospace, Orlando,
Florida, Interview, 5 August 1975.
- Hierholzer, Edward. Martin Marietta Aerospace,
Orlando, Florida, Interview, 14 August 1975.
- Integrated Circuits Catalog for Design Engineers.
Dallas, Texas: Texas Instruments Inc., n.d.
- Kellerman, Dave. Component Research Corporation.
Los Angeles, California, Telephone interview,
12 September 1975.
- Linear Integrated Circuits. Santa Clara, California:
National Semiconductor Corporation, 1975.
- Malmstadt, H.V., and Enke, C.G. Digital Electronics
For Scientists. New York: W.A. Benjamin Inc.
1964.
- Precision Resistors. Catalog. Malvern, Pennsylvania:
Vishay Resistive Group, 1975.

Renschler, Edward. Analog to Digital Conversion Techniques. Application Note 471. Phoenix, Arizona: Motorola Semiconductor Products Inc., 1971.

RCA Solid State '74 Data Book. Somerville, New Jersey: RCA Corporation, 1973.

Roberge, James K. Operational Amplifiers Theory and Practice. New York: John Wiley & Sons, Inc., 1975.

Siliconix Integrated Circuits Data Book. Santa Clara, California: Siliconix Inc., 1975.

Tobey, G.E.; Graeme, J.G.; and Huelsman, L.P., eds. Operational Amplifiers, Design and Applications. New York: McGraw Hill Book Company, 1971.

Transistors. Catalog. Santa Clara, California: National Semiconductor Corporation, 1975.